

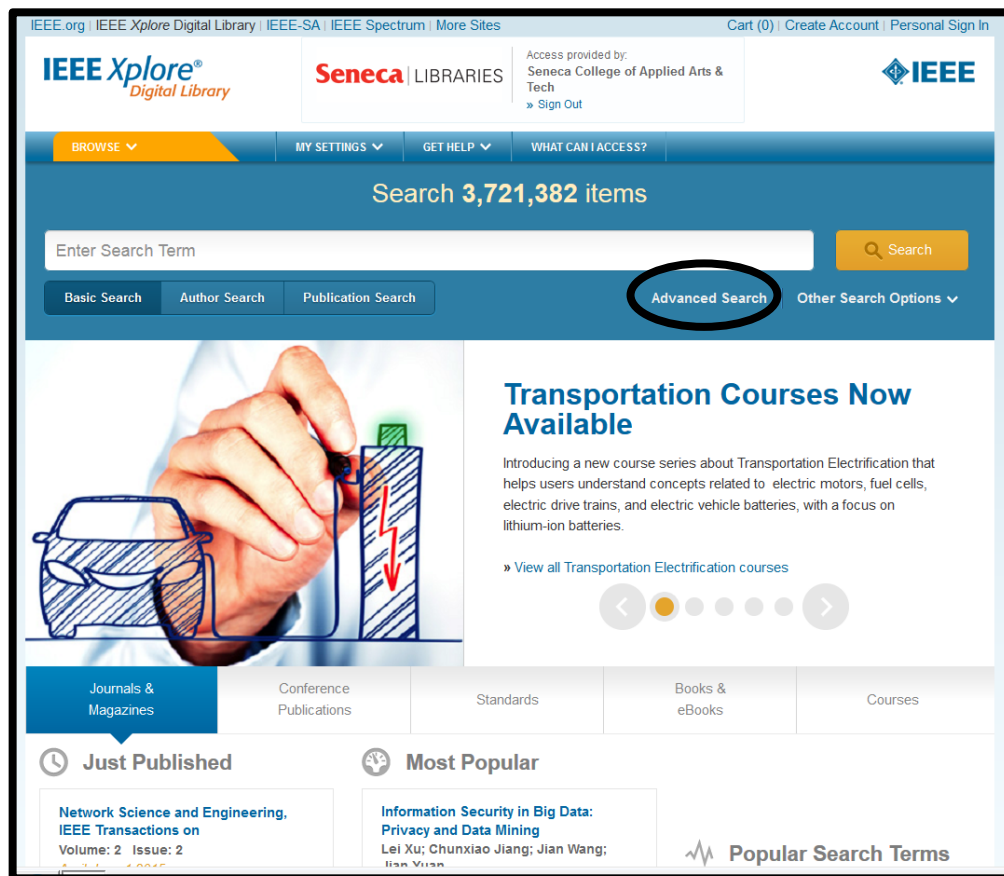
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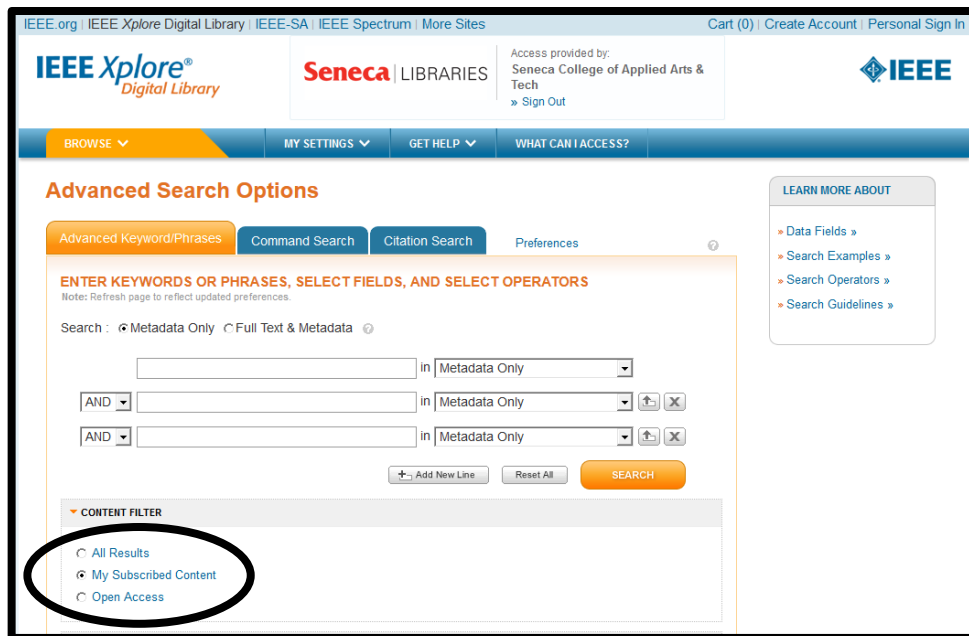
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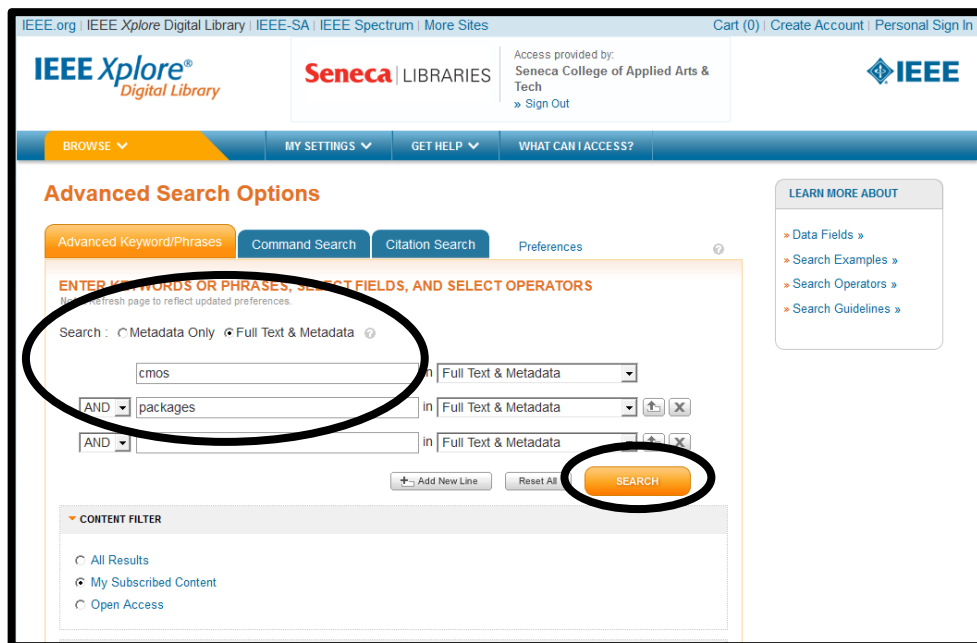


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New simultaneous switching noise analysis and modeling for high-speed and high-density CMOS IC package design

Publisher: IEEE

4 Author(s) Yungseon Eo ; W.R. Eisenstadt ; Ju Young Jeong ; Oh-Kyong Kwon [View All Authors](#)

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Abstract

Abstract: A new simple but accurate simultaneous-switching-noise (SSN) model for complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) package design was developed. Since the model is based on the sub-micron metal-oxide-semiconductor (MOS) device model, it can predict the SSN for today's sub-micron-based very large scale integration (VLSI) circuits. In order to derive the SSN model, the ground path current is determined by taking into account all the circuit components such as the transistor resistance, lead inductance, load capacitance, and oscillation frequency of the noise signal. Since the current slew rate is not constant during the device switching, a rigorous analysis to determine the current slew rate was performed. Then a new simple but accurate closed-form SSN model was developed by accurately determining current slew rate for SSN with the alpha-power-law of a sub-micron transistor drain current. The derived SSN model implicitly includes all the critical circuit performance and package parameters. The model is verified with the general-purpose circuit simulator, HSPICE. The model shows an excellent agreement with simulation even in the worst case (i.e., within a 10% margin of error but normally within a 5% margin of error). A package design methodology is presented by using the developed model.

Published in: IEEE Transactions on Advanced Packaging (Volume: 23 , Issue: 2 , May 2000)

Page(s): 303 - 312 **INSPEC Accession Number:** 6631951

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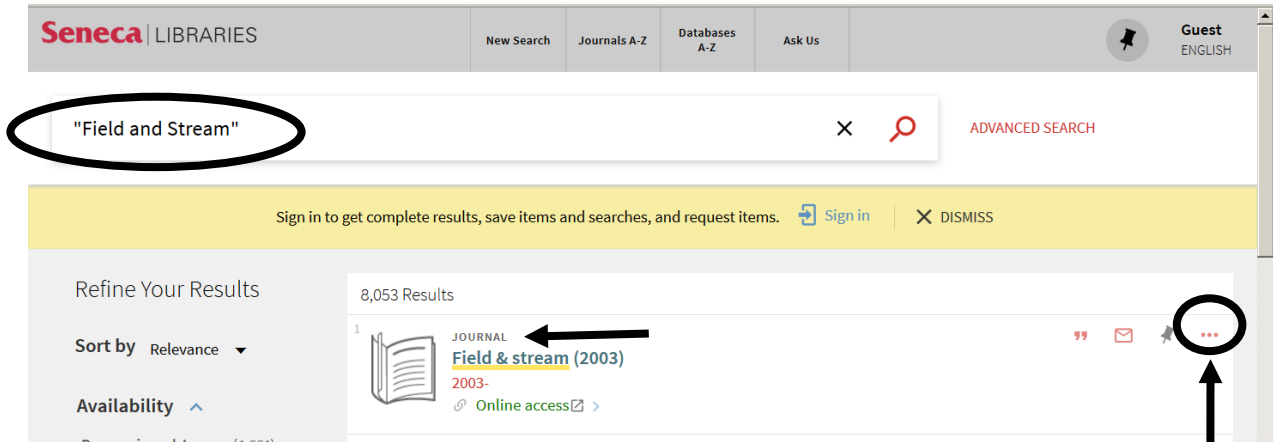
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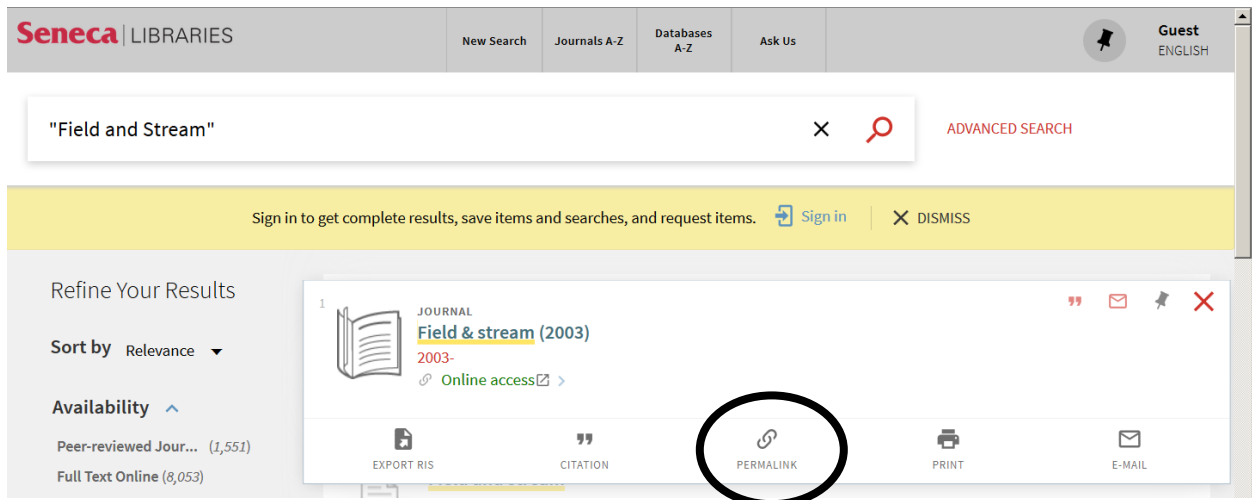
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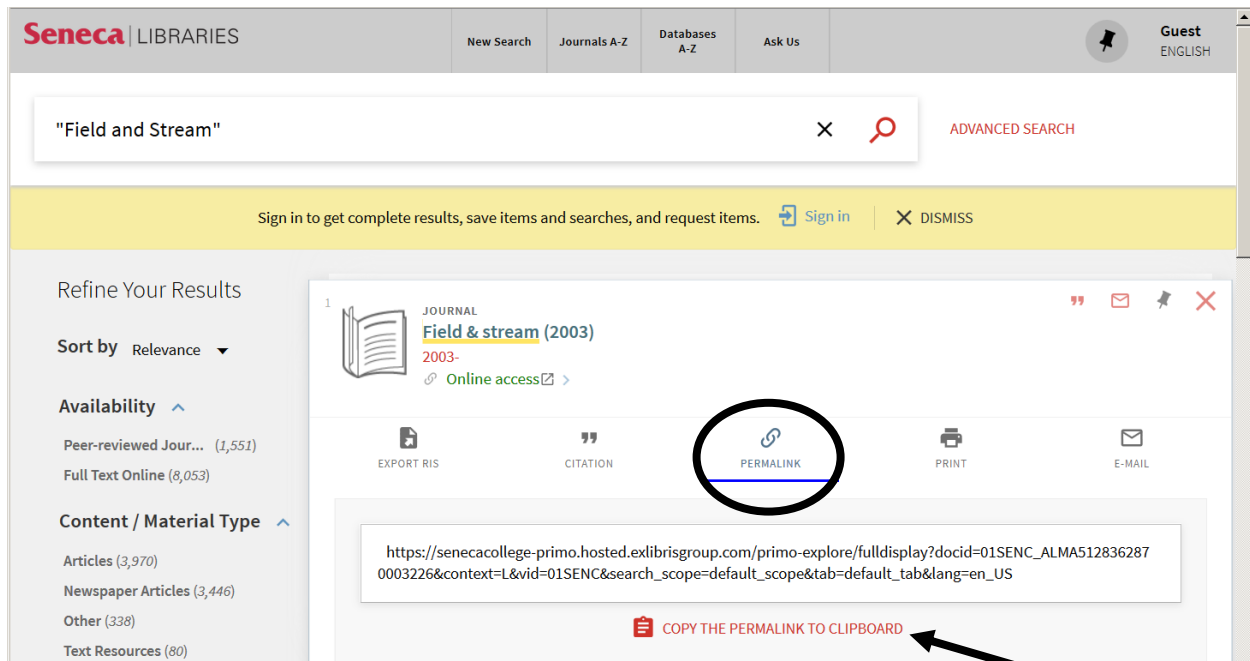


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